The latest activities related to the passive components in JAXA

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INTRODUCTION

In the present day, there are 95 models of passive and active components in Japan which meet the requirement of space components. They are qualified as JAXA qualified components by JAXA. Some of JAXA qualified components which have been gone through the review by ESA and met the criteria are included in the European Preferred Parts List (EPPL). These components contribute to the realization of rockets and space satellites, including commercial and government satellites. In recent years, the satellites which require lower cost and have shorter lifetime, called "New Space" satellites, are rapidly increasing. Although the high quality and high-cost components may not be required for such new space satellites, we believe the needs for space satellites are becoming polarized. The satellites will become larger as the space missions become more complex and more difficult. Such satellites should be accepting even fewer failures than the current satellites. Therefore, high-spec and high-quality components will be required even more.

In addition to the components which are qualified for space use, Commercial Off-The-Shelf (COTS) components are expected to apply to the latest space applications due to its advantage of performance and cost. However, since COTS components don't always have enough tolerance to space environment, their suitability for space application must be evaluated. Therefore, we have evaluated candidate COTS for space application to verify whether they have enough tolerance to the space environment. Based on the evaluation results, we establish guidelines for application of COTS components to spacecrafts. The guideline includes evaluation results, identified failure modes and precautions for use.

In this paper, we introduce the JAXA qualified passive components and latest revision of JAXA Qualification Test Specification (QTS) documents. And we also show the evaluation activity for the tolerance to the space environment of the passive COTS components in this paper.

Note that what they call "component" in Europe is called "part" in Japan ("Component" indicates "subsystem" in Japan). However, in this paper "component" is used for the same meaning as "part."

JAXA QUALIFIED PASSIVE COMPONENTS

There is a total of 95 models of JAXA qualified components, of which 78 models are passive components. Note that the PCBs and materials such as thermal control films are also included in JAXA qualified components. A list of JAXA qualified passive components and EPPL listed components are shown in Table 1.

Table 1. List of JAXA qualified passive components.

Comp. family	Description	Detail spec.	Manufacturer
Capacitors	MLCC EPPL	3(*1)	Murata
	Chip, Solid, Electrolytic, Tantalum EPPL	1	Matsuo Electric
Resistors	Chip, Thick Film EPPL	1	Tateyama Kagaku
		2	Hokuriku Electric
	Wire-Wound (Power Type)	2	Seiden Techno
		1	Sanada KOA
	Chip, Thin Film EPPL	1	Sanada KOA
Thermistors	Chip, Negative Temperature Coefficient EPPL	1	Tateyama Kagaku
	Lead, Negative Temperature Coefficient EPPL	1	Tateyama Kagaku
Fuses	Subminiature, Current-Limiting EPPL	1	Tateyama Kagaku
	Surface Mount, Miniature, Current-Limiting EPPL	1	Tateyama Kagaku
Temp. Sensors	Platinum EPPL	3	MHI(*2)
Osc. Crystals	Quartz Crystal Units	3	Nihon Dempa Kogyo
	Crystal Controlled Oscillators EPPL	1	Nihon Dempa Kogyo
Transformers and Inductors	Transformers, Power	8	Tamura
		1	Iriichi
	Coils	1	Iriichi
Wires and Cables	Differential Transmission Cables EPPL	2	Junkosha
Connectors	Rectangular, Miniature	1	JAE(*3)
		1	Nihon Maruko
	Rectangular, Miniature, High Density	1	JAE(*3)
		1	Nihon Maruko
	Rectangular, Microminiature EPPL	1	ITT Cannon
		1	Nihon Maruko
	Rectangular Miniature Mixed	1	Nihon Maruko
	Coaxial, RF	3	Waka Manufacturing
Printed Wiring Boards	Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	1	OKI Circuit Technology
	Fine Pitch Printed Wiring Boards, Glass Base Woven Epoxy Resin Base Material	1	EIGHT KOUGYO
		1	OKI Circuit Technology
		1	Meiko
	Fine Pitch Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	1	OKI Circuit Technology
		1	CMK
	Flexible, Polyimide Film Base Material	1	OKI Circuit Technology
	Rigid-Flexible	1	OKI Circuit Technology
	CIC Controlled Thermal Expansion, Glass Base Woven Polyimide Resin Base Material	1	OKI Circuit Technology
	Area Array Packaging	1	OKI Circuit Technology
	For High-speed Signals	1	OKI Circuit Technology

(*1) NASDA2040/L104(X7R)type and JAXA2040/M105(X7R) type only
(*2) MHI = Mitsubishi Heavy Industries
(*3) JAE = Japan Aviation Electronics Industry

As of July 2026, there are 15 passive component manufacturers which have abilities of manufacturing the products satisfy the requirements for space application defined by JAXA. In Table 1, components indicated in red are currently listed in EPPL. These components can be used for European space mission because their quality and the reliability have been already verified. Information about JAXA qualified components can be found in the JAXA EEE parts database [1]. The detail specifications and the applicable documents for all JAXA qualified components are available therein.

COMPARISON OF JAXA/ESCC QUALIFICATION TEST SPECIFICATION OF THE PASSIVE COTS COMPONENTS

JAXA qualified components are examined in the qualification test which are described in the generic and detail specification documents. As described in last SPCD presentation [2], there are three categories of specification documents in JAXA; General / basic specification called "JAXA-QTS-2000 [3]" defines basic requirements that are common for all component families. The generic specification defines common requirements for each component family. Detail requirements for each component family are defined in its detail specification. It has been verified that JAXA qualification system based on the above documents is equivalence to the ESCC (European Space Components Coordination) qualification system in the previous JAXA-ESA cooperation framework. The summary of the comparison results is shown in Table 2. The document tree of JAXA qualification system compared with that of ESCC qualification system is shown in Fig.1.

Table 2. Summary of JAXA and ESA qualified system comparison results

System	JAXA	ESCC
Basic document	JAXA-QTS-2000	-ESCC 20100 (component qualification) -ESCC 25400 (technology flow)
Subject	Manufacturing line	-Components (component qualification) -Manufacturing technology (technology flow)
Duration	3 years	2 years
Manufacturing line	Commercial lines may be used	Same as JAXA-QML system
Change control of QA program	Decision is made by TRB (Technology Review Board)	-Review and approved by ESCC (component qualification) -Same as JAXA-QML system (technology flow)
Test optimization	Decision is made by TRB Change must be described in the detail specification with rationale	-Restricted. Review / approval required by ESCC (component qualification) -Same as JAXA-QML system (technology flow)

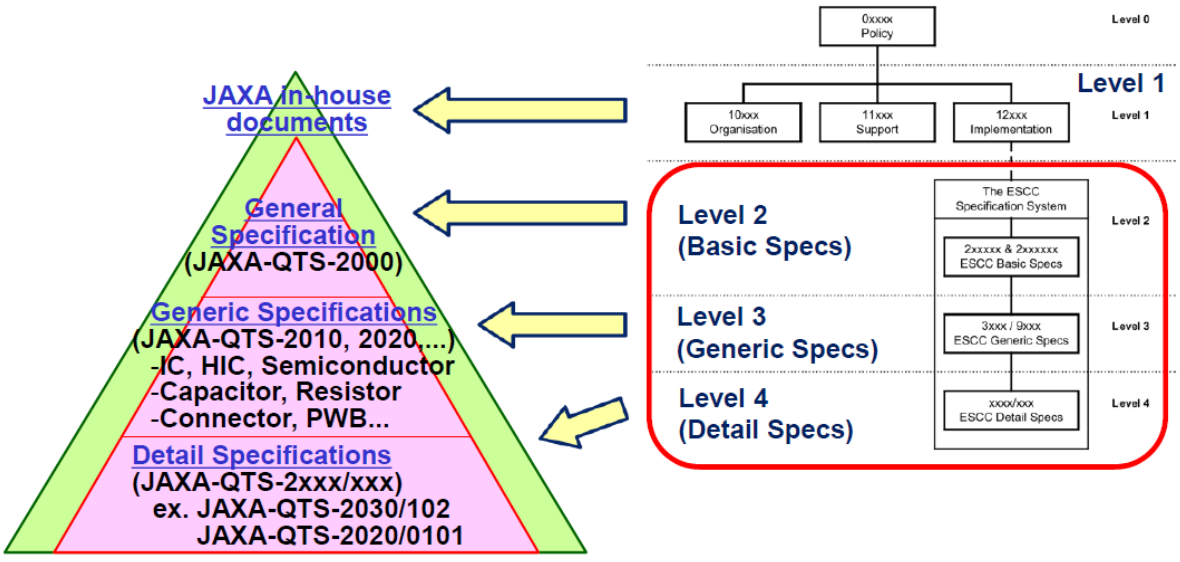


Fig. 1. Document tree of JAXA qualification system and ESCC qualification system

One major difference between the qualification system of JAXA and ESCC is that the basic requirements that are common for all component families are defined in one document (general specification (JAXA-QTS-2000)) [3] in JAXA qualification system. Another difference is that JAXA doesn't have its own specifications for test methods. The common requirements for each component family are defined in a generic specification. Detail requirements for each component are defined in its detail specification. Approval procedure for component qualification is defined in JAXA in-house documents. All the specifications are available through JAXA EEE parts database [1]. Duration of the certification is also different between JAXA/ESCC qualification systems. The certification is valid for 3 years in JAXA

qualification system whereas it is valid for 2 years in ESCC system. There is no other major difference when compared JAXA system with ESCC system.

Same comparison activity has been performing among the specification of DLA (Defence Logistics Agency) and the specification of JAXA and ESCC. Although there are some differences that come from the different background ideas, the equivalence was confirmed among the specification of DLA, ESCC and JAXA QTS.

JAXA ACTIVITY FOR QUALIFICATION SPECIFICATION

JAXA-QTS for JAXA qualified components have been revised periodically for the aim of keeping update, optimization and equivalence to other agency's specification such as MIL and ESCC as mentioned above. In addition, new appendix of QTS has been established before qualifying new type of components that has not been qualified in the past. In this section, representative topics of QTS revision and establishment of new edition of QTS and QTS appendix in FY2024 and FY2025 are introduced as a JAXA activity.

In FY2024, QTSs for platinum temperature sensors, crystal oscillators and thermistors have been revised.

Regarding the QTS-2180 [4] for platinum temperature sensors, revision was performed due to increasing of the requirement for longer operation lifetime geostationary satellites. Fig. 2 is one of the JAXA qualified platinum temperature sensors [5]. When platinum temperature sensors were qualified initially, qualification tests were set up assuming as platinum temperature sensors used in 10-years operation period of geostationary satellites. Recently, 15-years operation lifetime of geostationary satellites has been becoming common. Considering period in ground until launch to GEO, accelerated tests conditions of temperature cycling and humidity resistance in QTS-2180 were modified assuming to 20-years operation life of platinum temperature sensors.



Fig. 2. An example of the JAXA qualified platinum temperature sensors

For crystal oscillators, an exclusive QTS-2220 [6] for crystal oscillators was newly established. Fig 3 is the JAXA qualified crystal oscillator[7]. In the past, requirements for crystal oscillators were described in QTS-2020 [8] for hybrid ICs. Therefore, the qualification test (QT) and quality conformance inspection (QCI) requirements were not suitable for crystal oscillators. This was leading to higher products cost of qualified crystal oscillators. Refer to the MIL-PRF-55310 [9], the sample size of QT and QCI were reduced. In addition, a frequency-aging was added to screening as described in the ESCC3503 [10] to optimize test program for crystal oscillators.

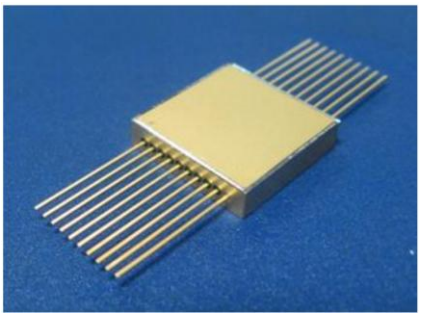


Fig. 3. The JAXA qualified crystal oscillator

Regarding revision of the QTS-2160 [11] for the thermistors, removing mechanical test items in the appendix A [12] of QTS-2160 was representative topic. The appendix A [12] of QTS-2160 is for chip negative temperature coefficient thermistors. Fig. 4 and Fig. 5 is a image [13] and schematic diagram of the JAXA qualified chip negative temperature coefficient thermistors, respectively. This appendix included mechanical stress tests such as shock, high frequency vibration and random vibration test. However, the chip negative temperature coefficient thermistor has no cavity as shown in Fig. 5, resulting in occurring no relative moving due to mechanical stress. Therefore, it was concluded that there are no concerns of failures caused by mechanical stress. Furthermore, variation of electrical characteristic which did not satisfy the criteria of mechanical stress was not identified during the mechanical stress test

in certified manufacturer. From the structure of the chip thermistors and test results in the past as mentioned above, mechanical stress test items were removed from appendix A [12] of QTS-2160 for chip negative temperature coefficient thermistors.

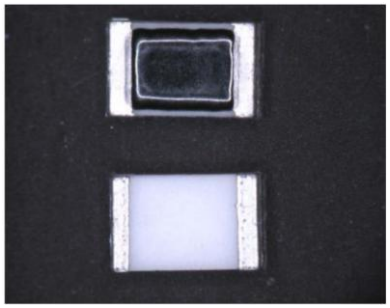


Fig. 4. The JAXA qualified thermistors, chip, negative temperature coefficient

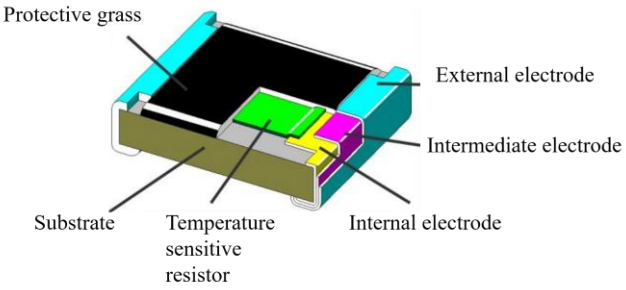


Fig. 5. Schematic diagram of chip negative temperature coefficient thermistors

In FY2025, we have revised QTSs for printed wiring boards, transformers and inductors, as well as connectors.

Regarding the revision of the QTS-2140 [14] for the printed wiring board (PWB), unclear descriptions in the QTS-2140 [14] were revised. Representative revision topics were hole diameter of test pattern for thermal stress test and evaluation of undercut at conductor. In the past, the specified through hole (TH) diameter of test pattern used for thermal stress test in the QCI was smaller than TH diameter of actual products. QCI requires thermal stress test that stress is more sever with increasing in TH diameter due to penetrating a lot of solder. Therefore, it is decided that TH diameter of test pattern for thermal stress test in the QCI should be specified as the maximum TH diameter of products. Regarding the undercut, necessity of the evaluating undercut was discussed. There are specific manufacturing methods that no undercut occurs. Therefore, it was decided that if undercut-free manufacturing method is adopted, observation of the undercut can be omitted from QCI. Note that in the case of QT, observation of the undercut has to be performed regardless manufacturing method as usual. In addition, revising QTS-2140 [14] for PWB was performed according to revising ESCC-Q-ST-70-60C [15]. ESA revised TH plating thickness measurement in the ESCC-Q-ST-70-60C [15] from a 3 points average calculation to minimum thickness measurement. According to this revision, the same revision of JAXA QTS-2140 [14] was performed to maintain equivalency to ESCC specification.

Regarding the revision of the QTS-2110 [16] for the transformers and inductors, adding test item, accommodating test condition to MIL specification and adding new type of inductor were representative topics. Fig. 6 is one of the JAXA qualified transformer [17]. In the past, while X-ray inspection was not specified in QTS-2110 [16], X-ray inspection was performed due to requirement from component user. According to opinion that X-ray inspection is necessary for verifying products workmanship and effects from environment test, X-ray inspection was added to after the thermal shock test for screening in the QT and QCI. In addition, it is found that life test duration in QTS-2110 [16] was shorter than one in the MIL-PRF-27 [18]. MIL-PRF-27 is a general specification for transformers and inductors. While minimum life test duration is 2016 hours in the MIL-PRF-27 [18], the duration in the QTS-2110 [16] was 2000 hours. For equivalent to MIL-PRF-27 [18], minimum life test duration in the QTS-2110 [17] was extended to 2016 hours. Furthermore, a new type of inductor specification was added to QTS-2110 [17]. This new type of inductor is surface mounted devise type with inward form lead. For qualifying this inductor in the future, specifications for the inductor which has such terminal structure and mounting construction will be added. Fig. 7 is the terminal structure of inward form lead. However, there is no established general method and condition of mechanical stress test for inward from lead such as terminal strength, shear and substrate bending. Therefore, the specifications of mechanical stress test for this lead type should be established before this type products will be qualified. This activity will be conducted after establishment of general mechanical stress test method and condition.

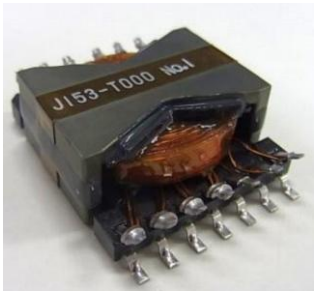


Fig. 6. An example of the JAXA qualified transformers

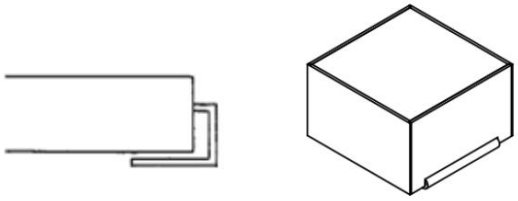


Fig. 7. Terminal structure of inward form lead

Regarding the revision of the QTS-2060 [19] for the connectors, appendix J of QTS-2060 for cable assemblies was newly established. In the past, only one side cable assembly was specified in the appendix F [20] of QTS-2060 for rectangular microminiature connectors. Fig. 8 is one of the JAXA qualified rectangular microminiature connector [21]. Based on the existing QTS for the connectors and ESCC for cable assemblies, newly appendix J for cable assemblies was established. It is specified that the connectors adopted for cable assemblies is rectangular microminiature connectors qualified in QTS-2060 appendix F. In terms of cables, radio frequency (RF) coaxial cables, fluorinated Ethylene Propylene (FEP) insulated wires, fluorinated polyimide insulated wires and differential transmission cables were adopted due to requirement from satellites manufacturers. It was specified these cables are selected from JAXA qualified components, MIL failure rate level S, R, D, C, GSFC S311 and ESCC level B, C. In addition, based on ESCC 3409 [22], QT and QCI test items were established. The QT for cable assemblies includes electrical measurements, shielding, vibration, temperature cycling, thermal stability and skew, external visual, DPA, crimp contact tensile strength and TID meanwhile the QT test items for connectors are excepted because the connector assembled to the cable has been already qualified.



Fig. 8. Examples of the JAXA qualified rectangular microminiature connectors

EVALUATION OF COTS COMPONENTS OF CHIP FILM CAPACITOR FOR APPLYING TO SPACE CRAFTS

As mentioned in the session of introduction, although using COTS components are expected to be the high performance and cost-reduction of spacecrafts, COTS components must be evaluated to verify whether they have enough tolerance to the space environment. We have conducted evaluation candidate COTS components, and established guidelines for application of COTS components to spacecrafts based on the evaluation results. We have completed to evaluate COTS of the flip chip IC, Polymer tantalum capacitor, the voltage-controlled crystal oscillator and the solid-state battery. To the next target, due to the demand of increasing electric power for spacecraft, we selected chip film capacitors with high rated voltage, large capacitance, small size and no voltage dependence of capacitance. In this section, evaluation results of film capacitor are introduced.

Samples under tests and test items

For evaluation of COTS component of chip film capacitor, we prepared components which were directly purchased from manufacturer. As shown in Fig. 9, the chip film capacitor is surface mount device, and it has stacking structure with alternating layers of dielectric and internal electrode. The characteristics of test sample is shown in Table 3.

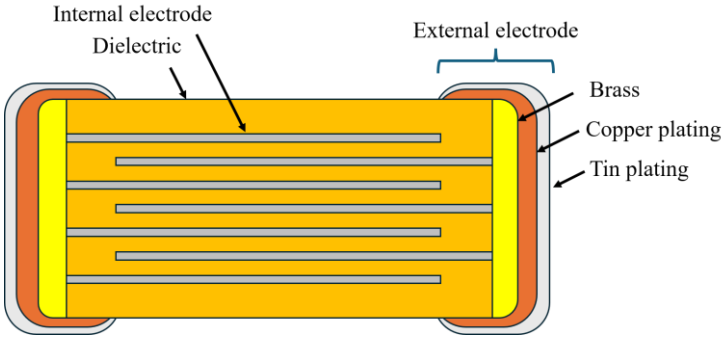


Fig. 9. Schematic diagram of chip film capacitor

Table 3. Characteristics of sample

Capacitor	Chip film capacitor
Chip size	4532
Rated voltage	16 V DC
Capacitance	4.7 μF
Tolerance of capacitance	±20%
Insulation resistance	At least 300 MΩ·μF
Dissipation factor	At most 1.5%
Operating temperature range	-55℃ ~ +125℃

The evaluation test items are shown in Table 4. This test flow is based on the qualification tests for MLCC in appendix M [23] of the JAXA-QTS-2040. Since JAXA does not have a specification for chip film capacitor at this time, this JAXA-QTS-2040 appendix M was referred. This is because the chip film capacitor has a similar stacking structure as MLCC and SMD same as MLCC. Regarding a part of test items, the detailed test conditions were accommodated to the characteristics of the chip film capacitor.

In this evaluation test, samples were mounted on substrate for measurement of electrical characteristics and application voltage during test. In the case of test items which do not need electrical measurements and applying voltage, test samples were not mounted on substrate. After the test, cross sectional analyses were performed for failure samples.

Table 4. Test items

Test			Sample size	Substrate mounting
Group	Order	Item		
I	1	Thermal shock and voltage aging	124ea	Mounted: 103ea No mounted: 21ea
	2	Insulation resistance (+125℃)		
	3	Dielectric withstanding voltage		
	4	Insulation resistance (+25℃)		
	5	Capacitance		
	6	Dissipation factor		
II	1	Externals	10ea	No mounted
	2	DPA		
III	1	Solderability	4ea	No mounted
	2	Resistance to soldering heat	4ea	Mounted
IV	1	Voltage-temperature characteristics	6ea	Mounted
	2	Moisture resistance		
V	1	Humidity, steady state, low voltage	6ea	Mounted
VI	1	Life	60ea	Mounted
VII	1	Barometric pressure	3ea	Mounted
VIII	1	Thermal shock and immersion cycling	9ea	Mounted
IX	1	Thermal shock	9ea	Mounted
X	1	Shear (destructive)	3ea	Mounted
	2	Substrate bending	3ea	Mounted

Test methods and results of the tests

a) Group I

In the Group I, to eliminate components has early failure, thermal shock and voltage aging were conducted on all 124 samples. In addition, electrical characteristics measurements were conducted before and after the thermal shock and the voltage aging. The thermal shock and voltage aging conditions and criteria are shown in Table 5. The electrical characteristics of all samples satisfied criteria before and after the thermal shock and the voltage aging. Results of the Group I test of representative samples before and after the test are shown in Table 6 and Table 7. In many samples, delamination of surface insulation film was observed as shown in Fig. 10. Fig. 10 is external image of S/N 111 that have the widest surface insulation film delamination. As a result of investigation, it was identified that such delamination occurred during the brush cleaning after the substrate mounting. Because the delamination was not caused by the thermal shock and the voltage aging test, the criterion of the external inspection was satisfied for all 124 samples. These 124 samples were assigned to Group II to Group X as shown in Table 4.

Table 5. The thermal shock and voltage aging conditions and criteria

Thermal shock condition	-Test method: MIL-STD-202 Method 107 -Temperature and duration: -55℃ (20 min)/+25℃ (5 min) /+125℃ (20 min) -Cycles: 100
Voltage aging condition	-Temperature: 125℃ -Applied voltage: 125% of rated voltage -Duration: 168 hours
Criteria	-Insulation resistance (+125℃): At least 64 MΩ -Withstanding voltage: No evidence of damage - Insulation resistance (+25℃): At least 64 MΩ -Capacitance: Within ±20% of 4.7μF -Dissipation factor: At most 1.5% -External inspection (only after the thermal shock and voltage aging): No evidence of mechanical damage

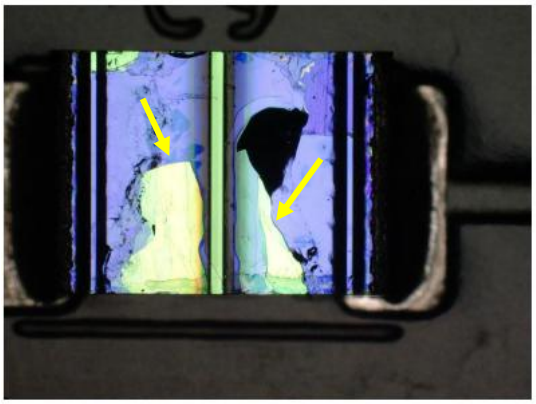


Fig. 10. The image of surface insulation film delamination of S/N 111

Table 6. Results of electrical characteristic before the thermal shock and the voltage aging

S/N	Insulation resistance (+125℃) [MΩ]	Withstanding voltage	Insulation resistance (+25℃) [MΩ]	Capacitance [μF]	Dissipation factor [%]
1	88,200	No damage	90,100	4.91	0.88
11	808,500	No damage	798,800	4.79	0.89
15	114,400	No damage	101,500	4.89	0.88
24	175,500	No damage	106,200	4.83	0.88
30	118,000	No damage	844,800	4.67	0.86
58	266,300	No damage	106,900	4.86	0.87
91	91,100	No damage	88,600	4.79	0.85
95	110,200	No damage	84,400	4.70	0.86
103	147,000	No damage	1,233,000	4.68	0.87
112	101,000	No damage	86,100	4.82	0.85
116	125,700	No damage	533,700	4.84	0.85

Table 7. Results of electrical characteristic and external inspection after the thermal shock and the voltage aging

S/N	Insulation resistance (+125℃) [MΩ]	Withstanding voltage	Insulation resistance (+25℃) [MΩ]	Capacitance [μF]	Dissipation factor [%]	External inspection
1	166,700	No damage	541,100	4.79	0.87	Appearance of delamination
11	388,800	No damage	313,500	4.66	0.88	Appearance of delamination
15	398,200	No damage	181,100	4.75	0.87	Appearance of delamination
24	120,500	No damage	211,700	4.70	0.93	Appearance of delamination
30	204,200	No damage	86,800	4.59	0.93	Appearance of delamination
58	157,500	No damage	99,500	4.75	0.92	Appearance of delamination
91	177,000	No damage	133,700	4.72	0.91	Appearance of delamination
95	96,500	No damage	115,900	4.62	0.92	Appearance of delamination
103	263,400	No damage	357,000	4.63	0.94	Appearance of delamination
112	252,700	No damage	161,300	4.75	0.94	Appearance of delamination
116	170,400	No damage	148,600	4.77	0.94	Appearance of delamination

b) Group II

In the Group II, external inspection, dimension measurement and DPA were conducted on 10 samples. Fig. 11 (a), (b), (c) are view from top, bottom and side images of representative sample S/N 1. In the Fig. 11 (a), (b), small peeling of surface insulation film was observed as indicated by yellow arrows. In the Fig. 11 (c), interlayer delamination was observed as indicated by yellow arrow. However, from Group I result, it is found that these external features have no effect on electrical characteristics. On the other hand, plating peeling and cracks that effect on electrical characteristics were not observed.

Results of material analyses by using a scanning electron microscope (SEM) and energy dispersive X-ray spectroscopy (EDX) in chip film capacitor are shown in Fig. 12 (a), (b). The observation results show that external electrodes which were plated by pure-Tin as described in Fig. 9. Therefore, conformal coating is needed to prevent growth of whisker for applying to spacecrafts [24].

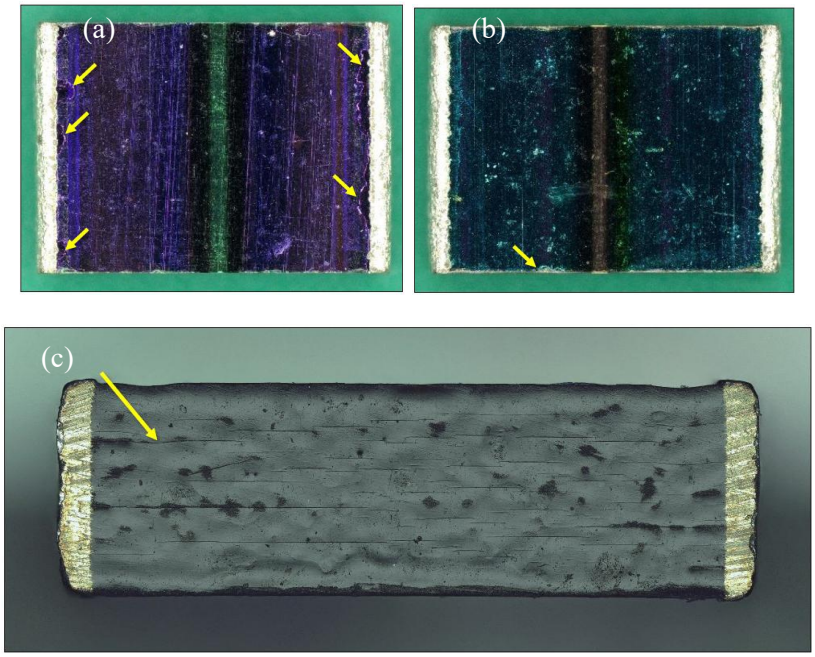


Fig. 11 top(a), bottom (b) and side(c) images of chip film capacitor S/N 1

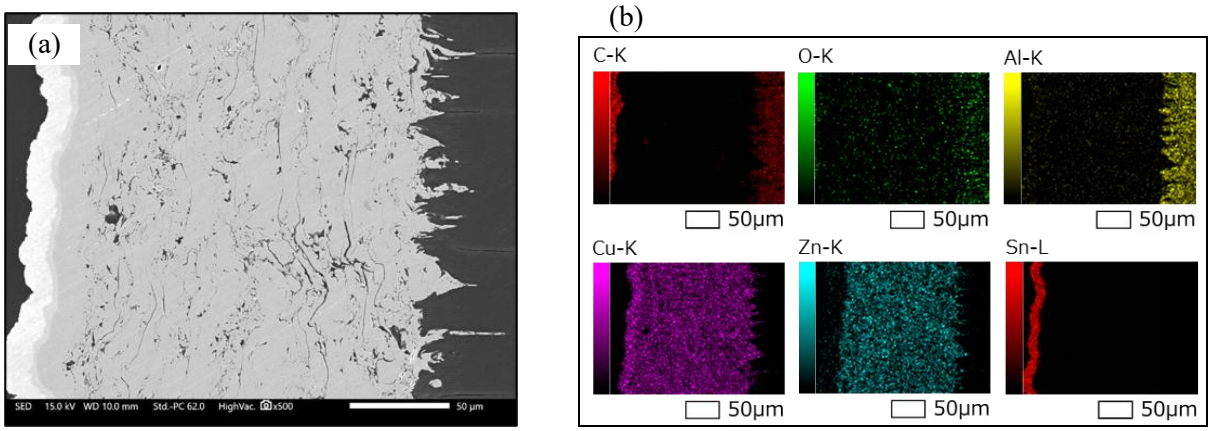


Fig. 12 Materials analyses area(a) and results of analyses(b) of chip film capacitor S/N 1

c) Group III

In the Group III, the solderability test and the resistance to soldering heat test were conducted on different test sample group. The S/N 11-14 and S/N 15-18 were assigned to the solderability and the resistance to soldering heat test, respectively.

The solderability test condition and criteria are shown in Table 8. Fig. 13 (a)-(d) are external view images of terminal electrode of the chip film capacitor after the solderability test. Symbols "-1" and "-2" is identifying external view images of one side and other side terminal, respectively.

The observation results of terminal electrode indicate that all of 4 samples showed satisfying criteria. Therefore, it was confirmed that the chip film capacitor has enough solderability.

Table 8. The solderability test condition and criteria

Test condition	-Test method: MIL-STD-202 Method 208 -Preconditioning: PCT 105°C, RH100%, storage for 4 hours -Flux: IPA solution with 25% of Rogin -Solder: Eutectic solder -Solder temperature: 230°C±5°C -Immersion time: 5±0.5 sec -Immersion rate: 25 mm/sec
Criteria	The terminal electrode surface should be covered by new solder at least 95%.

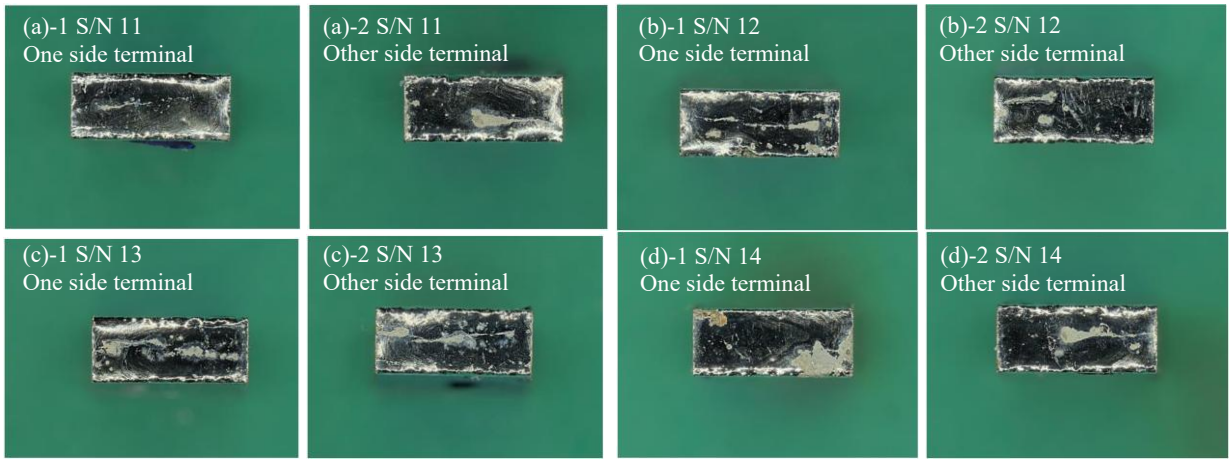


Fig. 13 (a)-(d). External inspection of terminal electrode of the chip film capacitor after the solderability test

The resistance to soldering heat test condition and criteria are shown in Table 9. Table 10 is results of electrical characteristic and external inspection after the resistance to soldering heat. Fig. 14 (a)-(d) are external view images of the chip film capacitor before and after the resistance to soldering heat test. Symbols "-1" and "-2" is identifying external view images before and after the test, respectively.

The measurement results of electrical characteristics after the resistance to soldering heat test satisfied the criteria. However, some delamination of the surface insulation film were observed in external observation. The red allows are indicating appearance of delamination. The yellow allows are indicating progress of delamination. As a result of investigation, these delamination are caused by not soldering heat stress but brush cleaning after the resistance to soldering heat test. Therefore, it was confirmed that the chip film capacitor has enough resistance to soldering heat.

Table 9. The resistance to soldering heat test condition and criteria

Test condition	-Test method: MIL-STD-202 Method 210 -Condition: B (DIP) -Solder: Eutectic solder -Solder temperature: 260℃±5℃ -Immersion time: 10±1 sec -Immersion rate: 25 mm/sec±6mm/sec
Criteria	-Insulation resistance at +25℃: At least 64 MΩ -Capacitance: Within ±7.5% of initial value -Dissipation factor: At most 1.5% -External: No evidence of mechanical damage, peeling or exposed internal electrodes and dissolution of electrodes

Table 10. Results of electrical characteristic and external inspection after the resistance to soldering heat

S/N	Insulation resistance (+25℃) [MΩ]	Capacitance change rate [%]	Dissipation factor [%]	External inspection
15	274,200	1.91	0.97	Appearance of peeling
16	559,600	2.06	0.96	Progress of peeling
17	222,100	1.91	0.98	Appearance of peeling
18	237,600	1.86	0.97	Progress of peeling

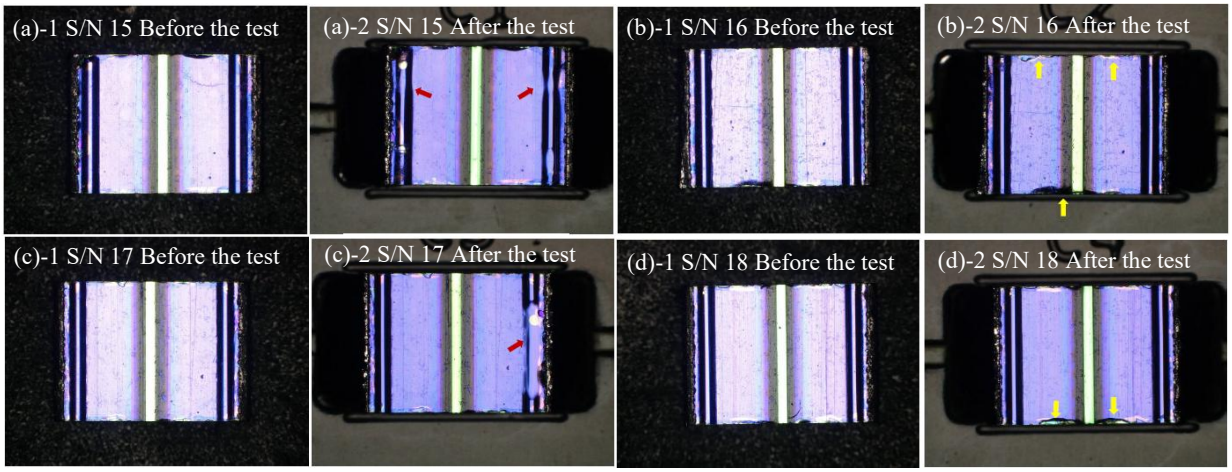


Fig. 14 (a)-(d). External images of the chip film capacitor before and after the resistance to soldering heat

d) Group IV

Evaluation tests in the Group IV were conducted on the same samples in the order of temperature characteristics and moisture resistance.

The measurement method of the temperature characteristics and criteria are shown in Table 11. The measurement results of the temperature characteristics are shown in Table 12. As shown in Table 12, all of 6 samples were satisfied criteria. It was confirmed that the chip film capacitor has satisfactory temperature dependence of capacitance.

Table 11. The measurement method of the temperature characteristics and criteria

Measurement method	-The order of temperature: +25℃→-55℃→+25℃ (Ref.) →+125℃ -Measurement voltage: 1 Vrms -Measurement frequency: 1 kHz
Criteria	-Capacitance: Within ±10% of value at +25℃(Ref.)

Table 12. Measurement results of the temperature characteristics

Measurement temperature	-55℃	+25℃(Ref.)	+125℃
S/N	Capacitance change from +25℃(Ref.) [%]	Capacitance [μF]	Capacitance change from +25℃(Ref.) [%]
19	-5.88	4.70	2.14
20	-5.99	4.83	2.11
21	-5.99	4.79	2.11
22	-5.97	4.68	2.14
23	-5.97	4.78	2.14
24	-6.00	4.75	2.12

The moisture resistance condition and criteria are shown in Table 13. The results of the moisture resistance were shown in Table 14. It is indicated that all samples failed in the insulation resistance at +25℃, relative change of capacitance from initial value and dissipation factor. It was confirmed that the chip film capacitor is sensitive to a pair of temperature cycling and moisture stress.

Table 13. The moisture resistance condition and criteria

Test condition	-Test method: MIL-STD-202 Method 106 -Temperature and humidity: Cycle between +65℃/95%RH and +255℃/95%RH -Duration: 24 hours/cycle -Total cycle: 20cycles -Applied voltage: Rated voltage during first 10 cycles
Criteria	-External: No evidence of mechanical damage -Insulation resistance at 25℃: At least 32 MΩ -Capacitance: Within ±10% of initial value -Dissipation factor: At most 1.5% -Withstanding voltage: No evidence of mechanical damage

Table 14. Results of electrical characteristic and external inspection after the moisture resistance

S/N	Insulation resistance [MΩ]	Capacitance change rate [%]	Dissipation factor [%]	Withstanding voltage	External inspection
19	13.74	14.08	1.955	No damage	No damage
20	11.91	13.79	1.817	No damage	No damage
21	11.71	13.63	1.985	No damage	No damage
22	12.24	13.91	1.855	No damage	No damage
23	10.68	14.10	2.024	No damage	No damage
24	7.36	14.04	1.878	No damage	No damage

Structural analysis was performed for one of failure sample to identify the cause of degrading electrical characteristics. Fig. 15 (a), (b) are a whole SEM image of failure sample and high magnification SEM image at

yellow square. Some delaminations were observed in the failure sample. Based on the result of structural analysis, it is estimated that degradation of electrical characteristics occurred as follows. During the test, the delamination was generated and then moisture penetrated into dielectric and the generated delamination. Furthermore, the temperature cycling facilitated moisture penetrating. The moisture induced electrical conduction, resulting in failure of insulation resistance and dissipation factor. In addition, the moisture caused additional capacitance, and then, this leads to the capacitance value exceeds the criterion.

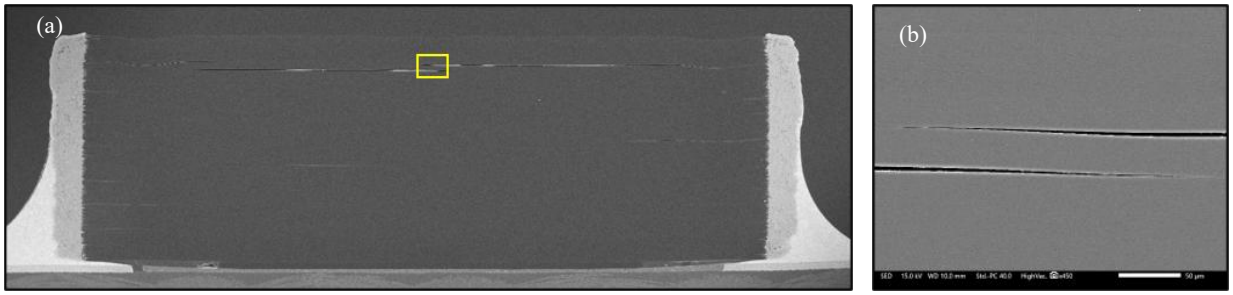


Fig. 15. SEM images of S/N 24 after the moisture resistance
(a)whole image, (b)high magnification image at yellow square of (a)

e) Group V

The humidity, steady state, low voltage was conducted on 6 samples.

The humidity, steady state, low voltage condition and criteria are shown in Table 15. The results of this test are shown in Table 16. It is indicated that relative change of capacitance from initial value was failure in all 6 samples. This degradation of capacitance without temperature cycling concluded that the chip film capacitor absorbs moisture easily and have high sensitivity to the moisture.

Table 15. The humidity, steady state, low voltage condition and criteria

Test condition	-Test method: MIL-STD-202 Method 103 -Temperature and humidity: +40℃/85%RH -Duration: 240 hours -Applied voltage: 1.3 V D.C.
Criteria	-Insulation resistance at 25℃: At least 64 MΩ -Capacitance: Within ±10% of initial value -External: No evidence of mechanical damage

Table 16. Results of electrical characteristic and external inspection after the humidity, steady state, low voltage

S/N	Insulation resistance [MΩ]	Capacitance change rate [%]	External inspection
25	14,670	13.80	No damage
26	16,680	13.42	No damage
27	14,440	13.80	No damage
28	16,290	13.65	No damage
29	17,150	13.74	No damage
30	16,140	14.11	No damage

f) Group VI

In Group VI, life test was conducted on 60 samples.

The life test condition and criteria were shown in Table 17. The measurement of electrical characteristics and external inspection were conducted after 1000, 2000, 3000, 4000 hours. Results of the insulation resistance after life test in S/N 58 were shown in Table 18. After 4000 hours, one of the 60 samples indicated failure. Characteristics of the insulation resistance at 125℃ was not satisfied in S/N 58. Results of the resistance measurement after life test in S/N 58 were shown in Table 18. Other electrical characteristics in S/N 58 were satisfied criteria. In addition, the electrical characteristics of other samples satisfied criteria. For comparison, trends of insulation resistance at 125℃ in representative samples were shown in Fig. 16. The broken red line in Fig. 16 identifies lower limit of insulation resistance at +125℃. All samples except S/N 58 showed insulation resistance at +125℃ of around 1500 MΩ after 4000 hours.

Table 17. The life test conditions and criteria

Test condition	-Test method: MIL-STD-202 Method 108 -Temperature: 125℃ -Applied voltage: Rated voltage -Duration: 4000 hours
Criteria	- Electrical measurement and external inspection point: After 1000, 2000, 3000, 4000 hours -Insulation resistance (+125℃): At least 19.2 MΩ -Insulation resistance (+25℃): At least 19.2 MΩ -Capacitance: Within ±20% of 4.7μF -Dissipation factor: At most 1.5% -External inspection: No evidence of mechanical damage

Table 18. Results of the insulation resistance after life test in S/N 58.

Insulation resistance at +125℃ [MΩ]			
1000 hours	2000 hours	3000 hours	4000 hours
82.1	30.2	20.5	17.4

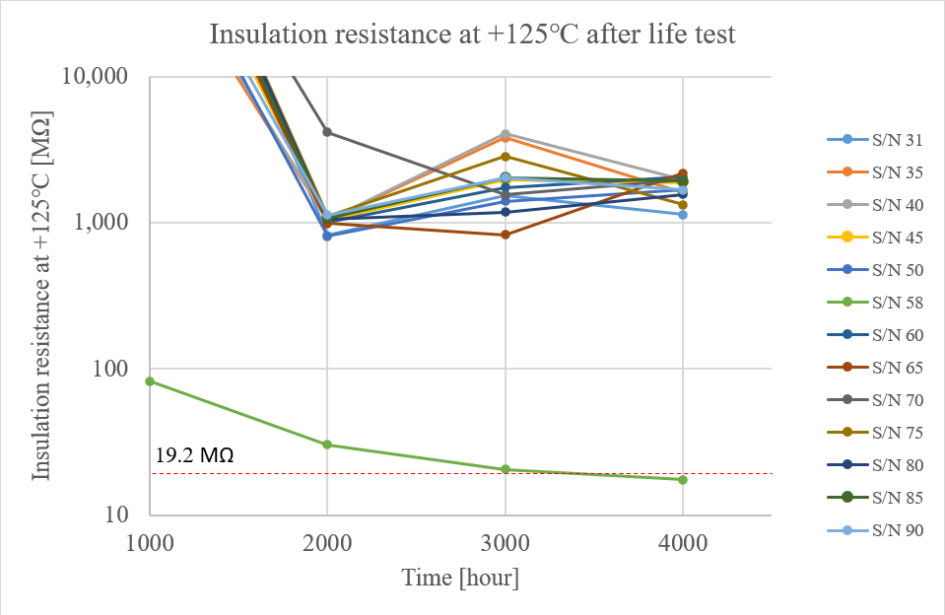


Fig. 16. Trend of the insulation resistance at +125℃ with life test duration.

Structural analyses were conducted on S/N 58 to identify the cause of degrading electrical characteristic. Fig. 17 (a) and (b) are whole cross section SEM image and high magnification image at yellow square, respectively. In high magnification image, delamination across multiple layers was observed. In S/N 58, it is estimated that this delamination was caused by long-term high temperature exposure, resulting in a failure of insulation resistance. It

is also considered that one of the possible causes of the appearance delamination is a deterioration of adhesion strength between interlayers due to thermal oxidation of dielectric during life test.

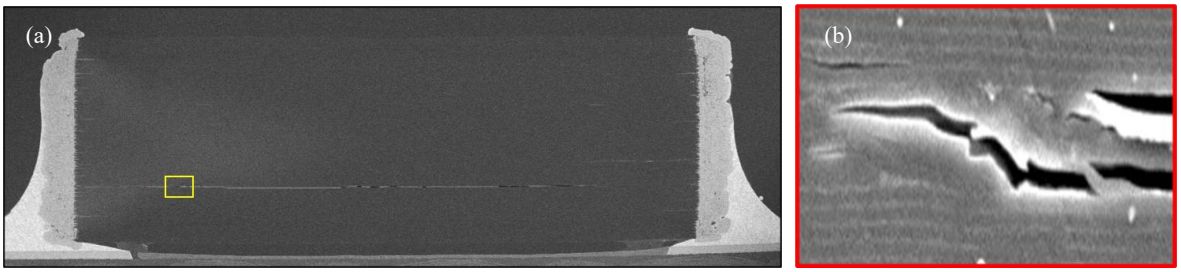


Fig. 17. Whole cross section SEM image(a) and high magnification image at yellow square(b) of S/N 58.

g) Group VII

The Barometric pressure test was conducted on 3 samples.
The barometric pressure test condition and criteria are shown in Table 19. Results of the barometric pressure test are shown in Table 20. No evidence of damage, arc discharge, electrical open and short was observed in all samples. Thus, it is confirmed that the chip film capacitor has resistance to low pressure environment.

Table 19. The barometric pressure test condition and criteria

Test condition	-Test method: MIL-STD-202 Method 105 -Pressure: 1.1 kPa -Applied voltage: 150% of rated voltage -Duration: 5±1 sec -Charge and discharge current: 50 mA
Criteria	-External: No evidence of damage, arc discharge, electrical open and short

Table 20. Results of the barometric pressure test

S/N	External inspection
91	No damage
92	No damage
93	No damage

h) Group VIII

The thermal shock and immersion cycle test were conducted on 6 samples.

The thermal shock and immersion cycle test condition and criteria are shown in Table 21. The electrical measurements and external inspection were conducted after the cleaning of salt crystal following immersion cycle. Results of the thermal shock and immersion cycle are shown in Table 22. The insulation resistance at 25℃ in all of 6 sample were failure.

Structural analysis was conducted on one of failure samples to identify the cause of degrading electrical characteristics. Fig. 18 (a) and (b) are whole cross section SEM image and high magnification image at yellow square, respectively. The delaminations between layers and across multiple layers were observed as indicated by red arrows. It is estimated that these delaminations caused by stress during the thermal shock and immersion cycle. Then, moisture penetrated into these delaminations and dielectric of the chip film capacitor during the immersion cycle, resulting in insulation resistance was failure. In addition, collapse of layers was observed at centre in the Fig. 18 (b). It is estimated that this collapse occurred when mechanical stress was applied during making cross section samples. It is estimated one of the causes of this that the interlayer bonding condition was deteriorated due to the thermal shock and immersion cycle stress.

From these results, it is confirmed again that the chip film capacitor is sensitive to moisture, as observed both moisture resistance test and the humidity, steady state, low voltage. Furthermore, it is confirmed that the interlayer bonding is sensitive to both temperature stress and humidity stress.

Table 21. The thermal shock and immersion cycle conditions and criteria

Thermal shock condition	-Test method: MIL-STD-202 Method 107 -Temperature and duration: -55℃ (20 min)/+25℃ (5 min) /+125℃ (20 min) -Cycles: 250
Immersion cycle condition	-Test method: MIL-STD-202 Method 104 -immersion cycle: Water at +65℃/saturated solution of sodium chloride at 25℃ -Duration: 15 min/15 min -cycle: 2 cycles
Criteria	-Withstanding voltage: No evidence of damage - Insulation resistance (+25℃): At least 32 MΩ -Capacitance: Within ±10% of initial value -Dissipation factor: At most 1.5% -External inspection: No evidence of mechanical damage

Table 22. Results of the thermal shock and immersion cycle test

S/N	Withstanding voltage	Insulation resistance (+25℃) [MΩ]	Capacitance change rate [%]	Dissipation factor [%]	External inspection
94	No damage	4.30	1.00	1.082	No damage
95	No damage	3.92	1.16	1.085	No damage
96	No damage	4.17	0.73	1.151	No damage
97	No damage	4.17	1.41	1.078	No damage
98	No damage	4.77	0.93	1.072	No damage
99	No damage	5.75	1.06	1.056	No damage
100	No damage	4.91	1.43	1.061	No damage
101	No damage	4.25	1.51	1.046	No damage
102	No damage	4.61	1.15	1.045	No damage

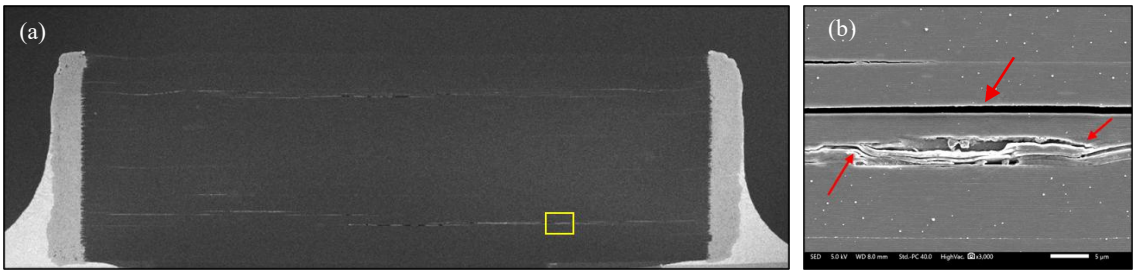


Fig. 18. Whole cross section SEM image(a) and high magnification image at yellow square(b) of S/N 95.

i) Group IX

The thermal shock test was conducted on 9 samples.

The thermal shock test condition and criteria are shown in Table 23. Results of the thermal shock test after 500 and 1000 cycle are shown in Table 24 and 25, respectively. All 9 samples satisfied criteria after 500 and 1000 cycle. This result indicates that the chip film capacitor has resistance to thermal shock.

Table 23. The thermal shock test condition and criteria

Test condition	-Test method: MIL-STD-202 Method 107 -Temperature and duration: -30℃(20 min)/+25℃(5 min) /+100℃(20 min) -Cycles: 1000
Criteria	-External inspection and electrical measurement point: After 500 and 1000 cycle -External inspection: No evidence of mechanical damage -Capacitance: Within ±10% of initial value -Insulation resistance at +25℃: At least 19.2 MΩ -Dissipation factor: At most 1.5% -Withstanding voltage: No damage

Table 24. Results of the thermal shock test after 500cycle

S/N	Insulation resistance [MΩ]	Capacitance change rate [%]	Dissipation factor [%]	Withstanding voltage	External inspection
103	92,300	-0.30	0.936	No damage	No damage
104	332	-0.28	0.915	No damage	No damage
105	439	-0.28	0.921	No damage	No damage
106	101,400	-0.29	0.916	No damage	No damage
107	534	-0.33	0.933	No damage	No damage
108	129,500	-0.28	0.926	No damage	No damage
109	365,300	-0.28	0.919	No damage	No damage
110	26,130	-0.29	0.929	No damage	No damage
111	152,300	-0.31	0.919	No damage	No damage

Table 25. Results of the thermal shock test after 1000cycle

S/N	Insulation resistance (+25℃)[MΩ]	Capacitance change rate [%]	Dissipation factor [%]	Withstanding voltage	External inspection
103	30,200	0.83	0.951	No damage	No damage
104	377.1	0.82	0.928	No damage	No damage
105	569.4	0.82	0.934	No damage	No damage
106	286,300	0.81	0.926	No damage	No damage
107	4,473	0.76	0.946	No damage	No damage
108	613,300	0.81	0.940	No damage	No damage
109	110,600	0.78	0.930	No damage	No damage
110	125,600	0.80	0.943	No damage	No damage
111	95,600	0.79	0.926	No damage	No damage

j) Group X

In Group X, shear test and substrate bending test were conducted on different sample group. The S/N 112-114 and S/N 115-117 were assigned to the shear test and the substrate bending test, respectively.

The shear test condition and criteria are shown in Table 26. Table 27 summarizes the shear modes. Results of the shear test are shown in Table 28. Fig. 19 (a)-(c) are observation results of electrodes left on substrate and chip film capacitor of S/N 112-114 after the shear test. Symbols “-1” and “-2” identify image of electrodes left on substrate and chip film capacitor, respectively. In Fig. 19 (a), (c), shear mode B identified in S/N 112 and 114 due to fracture marks on electrode were observed. Furthermore, shear mode D1 identified in S/N 113 due to detachment marks on solder were observed. However, the maximum load when chip film capacitor was sheared was larger than 5 N. Thus, it is considered that the chip film capacitor has enough shear strength.

Table 26. The shear test condition and criteria

Test condition	-Test method: JIS Z 3198-7 -Moving speed of test jig: 30 mm/min
Criteria	-Load: At least 5 N -Shear mode: Shear mode shall not be B or D1 in Table 27.

Table 27. Shear mode

Symbol	Shear mode
A	Sheared body
B	Separation between body and electrodes
C	Sheared solder
D1	Detachment of solder (from component surface)
D2	Detachment of solder (from board surface)
E	Peeling of the land on test board
F	Others

Table 28. Results of the shear test

S/N	Maximum load	Shear mode
112	121.34 N	B
113	92.26 N	D1
114	109.50 N	B

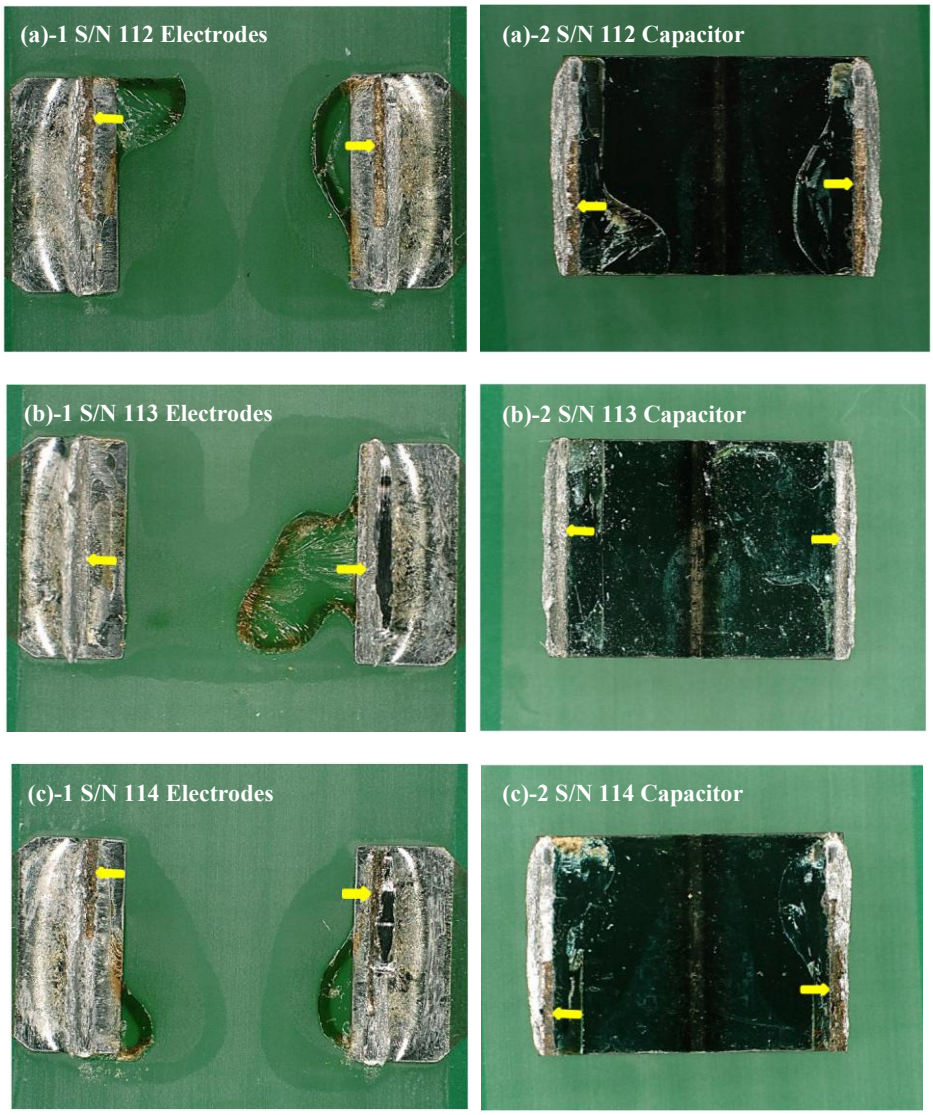


Fig. 19. Results of external observations of the electrodes left on substrate((a)-1, (b)-1, (c)-1) and chip film capacitor((a)-2, (b)-2, (c)-2) after shear test

The substrate bending test condition and criteria are shown in Table 29. Results of the substrate bending test are shown in Table 30. All of 3 samples indicated satisfying criteria. Thus, the chip film capacitor has resistance to substrate bending situations.

Table 29. The substrate bending test condition and criteria

Test condition	-Test method: JIS C 5101-1 -Flexure extent: 1 mm -Duration of pressure application: 5±1 sec
Criteria	-Capacitance during pressure application: Within ±10% of initial value -External inspection: No evidence of damage

Table 30. Results of electrical characteristic and external inspection after the substrate bending test

S/N	Capacitance change rate [%]	External inspection
115	0.036	No damage
116	0.141	No damage
117	0.082	No damage

Summary about evaluation of COTS chip film capacitor

We have evaluated chip film capacitor for future applications based on MLCC qualification test. From evaluation results, it is confirmed that chip film capacitor has resistance to solder mounting and mechanical stress required in space application. However, it is identified that evaluated chip film capacitor is sensitive to the moisture stress. In addition, it was found that one sample failed in insulation resistance at 125℃ measurement after 4000 hours life test. It is estimated that insulation resistance failure in life test was caused by delamination across multiple layers. Also, it is considered that one of the possible causes of the delamination across multiple layers is thermal oxidation of dielectric which deteriorates adhesion strength between interlayers. In preparation for using chip film capacitor in space application, we are considering to include evaluation results, related failure modes and precautions for use of chip film capacitor as COTS components for spacecraft to the technical data handbook of JERG-0-052 [25]. This handbook was established to contribute applying COTS to spacecraft due to explaining examples of evaluation COTS conducted in JAXA.

Based on evaluation results presented in this paper, we will evaluate 2 another types of film capacitors that have improved moisture resistance and suppress thermal oxidation. One type has different dielectric material which improves resistance of moisture. In addition, this type has a thicker design of dielectric. The thicker dielectric is expected to prevent delamination due to suppression of thermal oxidation. Other type has a protective package for resistance to moisture stress. After evaluations of these 2 types of film capacitor, we are also considering adding evaluation results and precautions for using in space applications to guideline which is mentioned above. Furthermore, if enough tolerant for space environment is confirmed in these film capacitors, we are considering qualifying these film capacitors.

OVERALL SUMMARY

In this paper, we introduced JAXA activities related to qualification system, qualified components and COTS components.

It was verified that the JAXA and ESA qualification system is equivalence through the previous JAXA-ESA cooperation framework.

The JAXA-QTS which is qualification specification for JAXA qualified components have been revised periodically for the aim of keeping update, optimization and equivalence to other agency's specification such as MIL and ESCC. In addition to this, new appendix of QTS has been established before qualifying new type of components. In FY2024, the QTSs for platinum temperature sensors, crystal oscillators and thermistors have been revised. And in FY2025, the QTSs for printed wiring boards, transformers and inductors, as well as connectors have been revised.

In parallel with these qualification components activity, COTS component which is expected to adapt to the space application has been evaluated. Chip film capacitor was selected for evaluation. It was verified that this component has enough resistance to solder mounting and mechanical stress required in space application. In addition, it is identified that evaluated chip film capacitor is sensitive to the moisture stress, and delamination which degrades insulation resistance was observed after the 4000 hours life test. Two other types of film capacitor which is expected to have resistance to moisture stress and to prevent appearance of delamination have been planning to evaluated to the next.

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